REMARKS

The Office action dated October 23, 2002 has been carefully considered. In the Office action, claims 1, 2, 10, 11, 15, 19-23, 30 and 31 were rejected under 35 U.S.C. § 102(e) as being anticipated by Diepstraten et al., U.S. Patent No. 6,243,736 (hereinafter Diepstraten). Claims 3-7, 9, 12, 13, 16, 17, 24-26, 28, 29, 32 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Diepstraten in view of Jennings, Jr., et al., U.S. Patent No. 5,542,088 (hereinafter Jennings). Claims 14 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Diepstraten in view of Borkenhagen et al., U.S. Patent No. 6,076,157 (hereinafter Borkenhagen). Claims 8 and 35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Diepstraten in view of Jennings and further in view of Borkenhagen. Claims 18 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Diepstraten in view of Jennings and further in view of Whiting et al., U.S. Patent No. 5,778,395 (hereinafter Whiting).

By the present amendment, claims 1-4, 10-12, 21, 24, 27-29 and 32 have been have been amended to more particularly point out and distinctly claim the subject matter of the invention, claims 36-44 have been added, and the rejections traversed as discussed below. Applicants submit that the amendments to the claims are unnecessary to distinguish the claimed subject matter from the prior art, and maintain that the claims recited patentable subject matter as filed and prior to amendment in view of the following remarks. Reconsideration is respectfully requested.

The present invention is generally directed towards a mechanism, in software, that limits the interference of a background process with another process, particularly a foreground process. The present invention is not a conventional CPU scheduler, but rather works external to such a

scheduler, and possibly in addition to a CPU scheduler. In fact, a primary reason that the invention is beneficial is that CPU schedulers do not schedule anything but CPU cycles, even though other resource (e.g., disk I/O) contention is frequently the reason that a background process interferes with a foreground process.

A background process is allowed to be executed for a brief time slice by a background task controller software component. When the task is executed, the actual performance of the background process is measured, and statistically analyzed with respect to its past performance data to determine whether the current performance is degraded relative to its past performance data, whether it is operating normally, or whether more information is needed. This measurement is not simply based on CPU cycles used, but factors in the actual relative performance, including any resource contention, and may based on various data such as the number of operations performed, the total time taken for those operations, and the relative amount of work performed by each operation.

Because the actual performance is dynamically measured for each execution period, contention for a resource other than the CPU is actively detected, enabling the background process to appropriately and quickly back off from interfering with the foreground process with respect to device contention.

If the measurement indicates that the performance is degraded relative to its past performance data, the background process is likely interfering with the foreground process. In this situation, the background process is then suspended for longer and longer time intervals (is backed off) between allowed executions, until either some acceptable limit is reached, or until the performance of the background process no longer appears to be degraded, which indicates that it is likely no longer interfering with another process. If normal performance is detected, the

back-off time interval is reset to some predetermined minimum value. If normal performance is detected or more information is needed, the task will again receive authorization to perform work. A critical task may have the suspension time dynamically adjusted based on its relative importance such that it will operate at a higher duty cycle. The measured performance data may be used to automatically and statistically calibrate a target performance value for determining whether the measured performance is degraded.

Note that the above description is for informational purposes only, and should not be used to interpret the claims, which are discussed below.

Turning to the rejections on the art, claims 1, 2, 10, 11, 15, 19-23, 30 and 31 were rejected as allegedly anticipated by Diepstraten. However, claim 1 recites at least two limitations not found in Diepstraten, including "receiving data indicative of a measured progress of the background task relative to past performance data," and "determining when to again execute the background task based on the data."

In contrast to claim 1, Diepstraten teaches a hardware-based context controller including context data for each of the background tasks, and a hardware-based background controller that reads the active or inactive statuses of the contexts to determine whether to switch in a background task during multitasking operations. This is an entirely different model than applicants' model as recited in claim 1.

First, it should be pointed out that the present invention as claimed is software-based, and thus has numerous advantages over the hardware architecture described in Diepstraten. For one, the present invention may be implemented on virtually any computing device without modification to its hardware. The mechanism described in Diepstraten requires custom hardware (including the context and background controllers) added to a computer system, which

is something that most computer users cannot benefit from. For this significant reason alone, the present invention is patentable over Diepstraten.

Moreover, in rejecting claim 1, the Office action has alleged that the Diepstraten teaches receiving data indicative of a measured progress of the background task, citing column 4, lines 5-7 of Diepstraten in support. However, column 4, lines 5-7 of Diepstraten are directed towards a status indicator that has only two states, namely a first state indicating that a background process is active, and thus should be given processor cycles from time to time, and a second state indicating that the background process is inactive and should not be run. Indeed, the status indicator of Diepstraten may be embodied in a flip-flop, a well-known hardware chip that toggles its voltage output between two states, off and on. *Diepstraten*, column 4, lines 21-24. Essentially the background task controller reads the status indicators to determine whether a background task should be executed or not. *Diepstraten*, column 4, lines 25-28.

Significantly, the status indicator of Diepstraten is not taught or suggested to be related to any measured progress of the background task relative to past performance data, nor anything that even relates to a progress measurement. There is no mention, let alone a fair teaching or suggestion of "measurement" or "progress" anywhere in Diepstraten. No reasonable interpretation of the status indicator can hold that this mechanism, which is essentially an on-off switch set by the background process, discloses, suggests or provides any motivation for "a measured progress of the background task relative to past performance data" as recited in claim 1. If the Office action maintains this rejection, then applicants specifically request a reasonably clear explanation and precise citation as to what in Diepstraten is alleged to be providing a progress measurement. In fact, Diepstraten teaches away from the present invention, by teaching that the background process of Diepstraten inactivates itself by way of the status indicator when

it does not have useful instructions to execute. *Diepstraten*, column 4, lines 14-15. This is not a progress measurement, which occurs when a background task is executing to perform useful work.

By law, in order to support an anticipation rejection, the Office action is required to show that each and every element of the claimed invention is disclosed in a single reference, and that each element is arranged as in the claim. Diepstraten, which simply does not disclose or in any suggest the concept of measured progress, let alone in a set of software components, clearly fails these requirements. As a result, the rejections are improper as a matter of law, and the claims (including those newly added) are patentable over Diepstraten. Reconsideration and withdrawal of the rejections of pending claims 1-7, and 10-14 based on Diepstraten is respectfully requested.

Turning to the rejection of claims 3-7, 9, 12, 13, 16, 17, 24-26, 28, 29, 32 and 33 as being unpatentable over Diepstraten in view of Jennings, applicants submit that like Diepstraten, Jennings also does not disclose or suggest at least the recited concept of a target progress and/or past performance data or the like. As such, any permissible combination of Diepstraten and Jennings would not make obvious the claimed subject matter.

Jennings is directed to a very different model than that of the present invention, in that Jennings teaches a user-controlled foreground-to-background swapping mechanism. In Jennings, a user sets up a user tolerance time indicative of how long the user is willing to wait for each application program command to complete. This user tolerance time is a user-defined time, with a default value of five seconds. In the event that the command will take more time that the user tolerance time, the task is moved from the foreground to a background manager, which may require user intervention via a dialog box.

Before pointing out how Jennings fails to disclose or suggest the claimed subject matter, applicants need to call attention to the fact that the any modification of Diepstraten with Jennings would render Diepstraten unsatisfactory for its intended purpose. Accordingly, the suggested modification / combination is impermissible. See MPEP § 2143.01. More particularly, Diepstraten is directed to a low-level hardware switching mechanism for CPU multitasking that operates at CPU-level cycle speeds to cyclically interleave foreground tasks with active background tasks, giving each an appropriate time slice of the CPU. The very purpose of Diepstraten is high-speed context activation in hardware. Diepstraten, column 4 lines 2-8; see also Diepstraten, column 2, lines 53-57, referring to context switching on the order of nanoseconds. A significant purpose of Diepstraten is to rapidly swap the contexts of the running task with the various other foreground and background tasks to improve multitasking efficiency.

In contrast, Jennings is referring to switching tasks to operate in the background based on user tolerance times on the order of five seconds, which may further include prompting the user for a decision. In Jennings, the calculation of whether to move a task to a background is not even performed until after a brief time-out period, and the calculation itself will need to use many processor cycles just to determine whether or not to move the task to a background. Modifying the background controller hardware of Diepstraten so as to perform such computations and comparisons before making a context switch, let alone possibly delay a context activation for millions of cycles so as to match human time considerations on the order of seconds, would make the background task controller of Diepstraten meaningless; the improvement in Diepstraten (that is provided via the status indicators that make the high-speed hardware manage tasks more efficiently) is simply not needed when tasks are only switched after

obtaining a time estimate as to their likely completion, and then comparing that time to a user-defined time to see if the switch is really needed, as in Jennings.

Moreover, in contrast to any of the claims, Jennings does not compare the estimated time required to complete an action with a past measurement or the like, and then use that measurement for throttling purposes. Instead, Jennings compares the estimated time required to complete an action against a user-defined tolerance time so to allow the user to do something else instead of waiting any longer. This is completely different than what is claimed, and the difference is significant. For one, past performance is not something that a user sets up, or leaves at a fixed default, but is instead an established value that is meaningful relative to the task and the system on which that task is run, not something that depends on a human's patience level.

Because each of the claims recite the concept of measured progress relative to some target progress (e.g., based on past performance data), all of the pending claims are patentable over Jennings, whether considered alone or in any permissible combination with Diepstraten. As such, applicants will not discuss the various claim rejections individually, with one exception. With respect to the rejections of claims 12 and 13, applicants note that the Office action cited FIG. 2 of Jennings as allegedly disclosing the recited automatic calibration of a target amount. FIG. 2 of Jennings is a user interface that shows what percentage of a task is complete. Applicants are unsure if this citation in the Office action is a typographical error, but if not, applicants request some reasonable explanation as to what is possibly being calibrated in this display, let alone how it ties into the concept of calibration as recited in the claim. Applicants submit that no reasonable interpretation of claim 12 and 13 are made obvious by this figure or its accompanying text.

To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art; (*In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)), and "all words in a claim must be considered in judging the patentability of that claim against the prior art;" (*In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)). Further, if prior art, in any material respect teaches away from the claimed invention, the art cannot be used to support an obviousness rejection. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed Cir. 1997). Moreover, if a modification would render a reference unsatisfactory for its intended purpose, the suggested modification / combination is impermissible. See MPEP § 2143.01

For at least the foregoing reasons, factual and legal, applicants submit that the present Office action has failed to establish *prima facie* obviousness as a matter of law with respect to any of the claimed subject matter. Reconsideration and withdrawal of the rejections of pending claims 3-7, 9, 12, 13, 16, 17, 24-26, 28, 29, 32 based on Diepstraten and/or Jennings is respectfully requested.

With respect to the rejections of claims 8, 14, 18, 27, 34 and 35 because the Diepstraten reference (and Jennings reference) were so seriously deficient with respect to the independent claims, applicants will not separately discuss these other dependent claims for purposes of brevity, except to submit that all of the claims are patentable for at least the foregoing reasons, and that these other dependent claims are patentable for additional reasons. As but one example, regarding the rejection of claim 8, applicants submit that column 15, lines 33-36 of Borkenhagen is not referring to exponentially doubling anything, let alone a suspend time, but is instead talking about one time being twice as long (or longer) as another latency time. No reasonable reading of column 15, lines 33-36 of Borkenhagen can hold that this teaches or suggests

increasing a suspend time by doubling a previous suspend time. Whiting is also irrelevant and non-analogous art.

Considering the obviousness rejections as a whole, to guard against the use of impermissible hindsight based on applicants' teachings, it is well settled that it is not permissible to combine references absent some teaching, suggestion, or motivation to combine the references. See, e.g., *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Geiger*, 815 F.2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987). In the present case, it appears that the Examiner can only have used impermissible hindsight based on applicants' own teachings to locate these disparate references, which simply do not go together, e.g., it is nonsensical to combine Diepstraten's high speed nanosecond-switching with Jennings' switching in human time frames measured in seconds.

In fact, the alleged motivation for combining these mismatched references are not based on anything found in the prior art or elsewhere, but are mere conclusory statements that are irrelevant to the prior art of record and/or to the claimed invention. For example, the unsupported reasons given for combining Diepstraten with Jennings of "measuring system efficiency and its performance to prevent application corruption of system failure" and "allows the system to focus on more important task to increase system performance" do not come close to the legal requirement of a showing of some teaching, suggestion, or motivation to combine the references. Instead of presenting any specific evidence of motivation to combine, the Office action has only made these conclusory statements, wholly unsupported by anything found in the references, in order to allege obviousness. However, such broad conclusory statements, standing alone, are not evidence of obviousness. *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614,

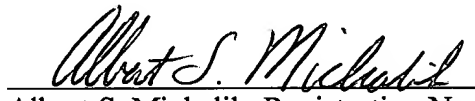
1617 (Fed. Cir. 1999). In the present application, the Office action has essentially done what is not proper by law, and used applicant's teachings as a blueprint, using an (incorrectly) modified Diepstraten for some of the claimed limitations, and, without any specific evidence of motivation to combine, has hunted for other references that might supply the limitations present in the application but missing from Diepstraten. Applicant submits that the § 103(a) rejections are thus improper as a matter of law for at least these additional reasons, and respectfully request withdrawal of the § 103(a) rejections.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that claims 1-44 of the present application are patentable over the prior art of record, and that the application is in good and proper form for allowance. Timely allowance is earnestly solicited.

If in the opinion of the Examiner a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney at (425) 836-3030.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this Amendment along with Transmittal, Petition for Extension of Time and Change of Correspondence Address in Application are being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date: April 22, 2003

Albert S. Michalik

1610 Amendment